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EXAMINER	
SHEW, JOHN	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,159	GOOCH, MARK	
	Examiner	Art Unit	
	John L. Shew	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7, 8, 9, 16, 17, 18, 19, 21, 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (Pub. No. US 2002/0116527 A1) in view of McAuley et al (Patent No. 5386413).

Claim 1, Chen teaches a method for parallel hash transformation in a network device (Fig. 1, page 1 para. [0002]-[0005]) referenced by the network device using a lookup engine of N parallel Hardware Hash Functions 102, to generate a hash pointer (Fig. 1, page 1 para. [0005]) referenced by the N r-bit hash value outputs of the hardware hash functions, for an address input (Fig. 1, page 1 para. [0005]) referenced by the 97-bit layer-4 address <DA,SA,DP,SP,PRO>, comprising receiving an address input (Fig. 1, page 1 para. [0005]) referenced by the arrival of the address 101 for processing by the N different hardware hash functions 102, apportioning the address input among a plurality of hashing units (Fig. 4, page 3 para. [0048]-[0049]) referenced by the Partition

the address Step 302 for hashing by the SHIFT/XOR operation for each segment, executing a hash transformation on the apportioned address inputs in parallel (Fig. 1, page 1 para. [0002]-[0005) referenced by the parallel Hardware Hash Functions 102 operating on the input address lookup request, resulting in a corresponding plurality of hashing unit outputs (Fig.1, page 1 para. [0002]-[0005) referenced by the N r-bit hash values from the N hardware hash functions 102. Chen does not teach combining the hashing unit outputs to generate a hash result corresponding to the address.

McAuley teaches combining the hashing unit outputs to generate a hash result corresponding to the address input (col. 3 lines 60-66, Fig. 5, col. 9 lines 21-43) referenced by the Content Addressable Memory modules 110 111 112 performing HASH after the Mask Circuit which blocks part of the destination address wherein each of the outputs 140 141 142 goes to a Prioritizer 150 for combining the outputs based on a priority flag.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of CAM for routing table lookup of MaAuley to the input address lookup engine of Chen for the purpose of providing a switch memory for implementing a multilevel hierarchical routing table as suggested by McAuley (col. 5 lines 22-24).

Claim 7, Chen teaches wherein the network device is a router (page 1 para. [0017]) referenced by the layer-3 router for generating a forwarding decision, configured to use the hash result for storing routing addresses with a routing table (Fig. 2, page 1 para.

[0018], Fig. 3, page 3 para. [0052]-[0054]) referenced by the hash Flow Table 121 results to the CPU 13 for rules determination entry to the Routing Table 141.

Claim 8, Chen teaches wherein the network device is a switch (page 1 para. [0017]) referenced by the layer-2 switch for generating a forwarding decision, configured to use the hash result for storing forwarding addresses with a forwarding table (Fig. 2, page 1 para. [0018], Fig. 3, page 3 para. [0052]-[0054]) referenced by the hash Flow Table 121 results to the CPU 13 for rules determination entry to the Filtering Table 181.

Claim 9, Chen teaches a parallel hash transformation system (Fig. 1, page 1 para. [0002]-[0005]) referenced by the network device using a lookup engine of N parallel Hardware Hash Functions 102, for generating a hash pointer (Fig. 1, page 1 para. [0005]) referenced by the N r-bit hash value outputs of the hardware hash functions, for an address input (Fig. 1, page 1 para. [0005]) referenced by the 97-bit layer-4 address <DA,SA,DP,SP,PRO>, comprising an input configured to accept an address (Fig. 1, page 1 para. [0005]) referenced by the arrival of the address 101 for processing by the N different hardware hash functions 102, a plurality of parallel hash units coupled to the input to receive respective portions of the address (Fig. 3, Fig. 4, page 3 para. [0048]-[0049]) referenced by the Partition the address Step 302 for hashing by the parallel SHIFT/XOR operation for each segment by the Shift Control Logic 22, the hashing units configured to execute a hash transformation on the respective portions of the address in parallel (Fig. 3, Fig. 4, page 3 para. [0048]-[0049]) referenced by address segments [illegible] referenced by the N r-bit hash value outputs of the hardware hash [illegible], for [illegible] the 97-bit layer-4 address [illegible]

input to the parallel hashing function of the Shift Control Logic 22, and generate respective hash outputs (Fig. 3) referenced by the output of the respective hashing Shift Control Logic units 22. Chen does not teach a combination unit coupled to receive the respective hash outputs.

McAuley teaches a combination unit coupled to receive the respective hash outputs (col. 3 lines 60-66, Fig. 5, col. 9 lines 21-43) referenced by the Content Addressable Memory modules 110 111 112 performing HASH after the Mask Circuit which blocks part of the destination address wherein each of the outputs 140 141 142 goes to a Prioritizer 150, the combination unit configured to combine the respective hash outputs into a hash result (col. 3 lines 60-66, Fig. 5, col. 9 lines 21-43) referenced by the outputs 140 141 142 going to a Prioritizer 150 for combining the outputs based on a priority flag, and an output configured coupled to the combination unit to transmit the has result (Fig. 5) referenced by the transmission of the prioritized output on Port B 102.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of CAM for routing table lookup of MaAuley to the input address lookup engine of Chen for the purpose of providing a switch memory for implementing a multilevel hierarchical routing table as suggested by McAuley (col. 5 lines 22-24).

Claim 16, Chen teaches wherein the system is implemented within a router (page 1 para. [0017]) referenced by the layer-3 router for generating a forwarding decision, configured to use the hash result for storing routing addresses with a routing table (Fig.

2, page 1 para. [0018], Fig. 3, page 3 para. [0052]-[0054]) referenced by the hash Flow Table 121 results to the CPU 13 for rules determination entry to the Routing Table 141.

Claim 17, Chen teaches wherein the system is implemented within a switch (page 1 para. [0017]) referenced by the layer-2 switch for generating a forwarding decision, configured to use the hash result for storing routing addresses with a routing table (Fig. 2, page 1 para. [0018], Fig. 3, page 3 para. [0052]-[0054]) referenced by the hash Flow Table 121 results to the CPU 13 for rules determination entry to the Routing Table 141.

Claim 18, Chen teaches a result storage register for storing the hash result coupled to a unit (Fig. 1, page 1 para. [0004]-[005]) referenced by the Comparator 103 which receives the output of the Hardware Hash 102, the result storage register configured to transmit the hash result to a unit to enable a successive hash transformation on successive address inputs (Fig. 1, page 1 para. [0004]-[005]) referenced by the Comparator 103 outputs to a Multiplexer 105 for each respective hash address calculation and an OR unit to enable a Hit of a hash transaction. Chen does not teach a combination unit.

McAuley teaches a combination unit (col. 3 lines 60-66, Fig. 5, col. 9 lines 21-43) referenced by the Prioritizer receiving the outputs of the CAM modules 140 141 142.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of CAM for routing table lookup of MaAuley to the input address lookup engine of Chen for the purpose of providing a switch memory for

implementing a multilevel hierarchical routing table as suggested by McAuley (col. 5 lines 22-24).

Claim 19, Chen teaches in a network device (Title) referenced by a network device, a system for performing a parallel hash transformation (Fig. 1, page 1 para. [0002]-[0005]) referenced by the network device using a lookup engine of N parallel Hardware Hash Functions 102, comprising means for receiving an address input (Fig. 1, page 1 para. [0005]) referenced by the arrival of the address 101 for processing by the N different hardware hash functions 102, means for dividing the address input among a plurality of hashing units (Fig. 3, Fig. 4, page 3 para. [0048]-[0049]) referenced by the Partition the address Step 302 for hashing by the parallel SHIFT/XOR operation for each segment by the Shift Control Logic 22, means for executing a hash transformation on the apportioned address inputs in parallel (Fig. 3, Fig. 4, page 3 para. [0048]-[0049]) referenced by address segments input to the parallel hashing function of the Shift Control Logic 22, resulting in a corresponding plurality of hashing unit outputs (Fig. 3) referenced by the output of the respective hashing Shift Control Logic units 22. Chen does not teach means for combining the hashing unit outputs. McAuley teaches means for combining the hashing unit outputs to generate a hash result corresponding to the address input (col. 3 lines 60-66, Fig. 5, col. 9 lines 21-43) referenced by the Content Addressable Memory modules 110 111 112 performing HASH after the Mask Circuit which blocks part of the destination address wherein each

of the outputs 140 141 142 goes to a Prioritizer 150 for combining the outputs based on a priority flag.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of CAM for routing table lookup of MaAuley to the input address lookup engine of Chen for the purpose of providing a switch memory for implementing a multilevel hierarchical routing table as suggested by McAuley (col. 5 lines 22-24).

Claim 21, Chen teaches wherein the network device is a router (page 1 para. [0017]) referenced by the layer-3 router for generating a forwarding decision, configured to use the hash result for storing routing addresses with a routing table (Fig. 2, page 1 para. [0018], Fig. 3, page 3 para. [0052]-[0054]) referenced by the hash Flow Table 121 results to the CPU 13 for rules determination entry to the Routing Table 141.

Claim 22, Chen teaches wherein the network device is a switch (page 1 para. [0017]) referenced by the layer-2 switch for generating a forwarding decision, configured to use the hash result for storing routing addresses with a routing table (Fig. 2, page 1 para. [0018], Fig. 3, page 3 para. [0052]-[0054]) referenced by the hash Flow Table 121 results to the CPU 13 for rules determination entry to the Routing Table 141.

Claim 23, Chen teaches further comprising means for storing the hash result coupled to multiplexer means (Fig. 1; page 1 para. [0004]-[005]) referenced by the Comparator 103 which receives the output of the Hardware Hash 102, the storing means configured to

transmit the hash result to multiplexer means to enable a successive hash transformation on successive address inputs (Fig. 1, page 1 para. [0004]-[005]) referenced by the Comparator 103 outputs to Multiplexer 105 for each respective hash address calculation and an OR unit to enable a Hit of a hash transaction. Chen does not teach a combining means.

McAuley teaches means for combining the hashing unit outputs to generate a hash result corresponding to the address input (col. 3 lines 60-66, Fig. 5, col. 9 lines 21-43) referenced by the Content Addressable Memory modules 110 111 112 performing HASH after the Mask Circuit which blocks part of the destination address wherein each of the outputs 140 141 142 goes to a Prioritizer 150 for combining the outputs based on a priority flag.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of CAM for routing table lookup of MaAuley to the input address lookup engine of Chen for the purpose of providing a switch memory for implementing a multilevel hierarchical routing table as suggested by McAuley (col. 5 lines 22-24).

Claims 2, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and McAuley as applied to claims 1, 9 above, and further in view of Donoghue et al. (Pub. No. US 2003/0117944 A1).

Claim 2, Chen teaches a lookup engine for network devices with a parallel hashing function adaptable to layer-2, layer-3 and layer-4 switch, router or bridge (page 1 para. [0017]). Chen and McAuley do not teach the input address is a 48-bit address input. Donoghue teaches an input address is a 48-bit address input (Fig. 4, page 5 para. [0070]) referenced by the layer 2 MAC address section is a 48-bit form.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the 48-bit layer-2 structure of Donoghue to the input address lookup engine of Chen and McAuley for the purpose of providing a versatile control path by means of which units in a cascade connection can exchange control information as suggested by Donoghue (page 1 para. [0009]).

Claim 10, Chen teaches wherein the input is configured to accept a layer-2 address input and the address input is respectively apportioned among the parallel hash units (Fig. 1, page 1 para. [0017]) referenced by the hashing mechanism adapted to a layer-2 switch and the input address 101 is partitioned between parallel Hardware Hash units 102 1-N. Chen and McAuley do not teach the input address is a 48-bit address input. Donoghue teaches an input address is a 48-bit address input (Fig. 4, page 5 para. [0070]) referenced by the layer 2 MAC address section is a 48-bit form.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the 48-bit layer-2 structure of Donoghue to the input address lookup engine of Chenand McAuley for the purpose of providing a versatile control path by

means of which units in a cascade connection can exchange control information as suggested by Donoghue (page 1 para. [0009]).

Claims 3, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, McAuley and Donoghue as applied to claims 1, 2, 9, 10 above, and further in view of Glaise et al. (Patent No. 6097725).

Claim 3 Chen, McAuley and Donoghue teach a lookup engine for network devices for MAC addresses. Chen, McAuley and Donoghue do not teach the hash result is a 12-bit hash result.

Glaise teaches a hash result is a 12-bit hash result (Fig. 14, col. 7 lines 50-64) referenced by the CPI/VCI field value entered is multiplied by the matrix with the result being a 12 bit vector used as a hash key.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the hash matrix to 12-bit result of Glaise to the input address lookup engine of Chen, McAuley and Donoghue for the purpose of providing a low cost method and device for implementing a searching function where processing time is limited as suggested by Glaise (col. 2 lines 61-63).

Claim 11 Chen, McAuley and Donoghue teach a lookup engine for network devices for MAC addresses. Chen, McAuley and Donoghue do not teach the hash result is a 12-bit hash result.

Glaise teaches a hash result is a 12-bit hash result (Fig. 14, col. 7 lines 50-64) referenced by the CPI/VCI field value entered is multiplied by the matrix with the result being a 12 bit vector used as a hash key.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the hash matrix to 12-bit result of Glaise to the input address lookup engine of Chen, McAuley and Donoghue for the purpose of providing a low cost method and device for implementing a searching function where processing time is limited as suggested by Glaise (col. 2 lines 61-63).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and McAuley as applied to claim 1 above, in view of Hunter et al. (Pub. No. US 2002/0059197 A1).

Claim 4, Chen teaches a lookup engine for network devices with a parallel hashing function adaptable to layer-2, layer-3 and layer-4 switch, router or bridge (page 1 para. [0017]). Chen and McAuley do not teach the input address is a 128-bit address input.

Hunter teaches an input address is a 128-bit address input (page 1 para. [0006], page 2 para. [0035]) referenced by the Layer 3 address using the IP protocol which is 128-bit address for IPv6.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the 128-bit layer-3 address of Hunter to the input address lookup engine of Chen and McAuley for the purpose of locating an entry in a forwarding database using an improved longest match search as suggested by Hunter (page 2 para. [0017]).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, McAuley and Hunter as applied to claims 1, 4 above, and further in view of Melvin (Patent No. 6804767).

Claim 5, Chen, McAuley and Hunter teach a lookup engine for network devices for 128-bit IPv6 addresses. Chen, McAuley and Hunter do not teach the hash result is a 20-bit hash result.

Melvin teaches a hash result is a 20-bit hash result (Fig. 10, col. 8 lines 34-54) referenced by the hash function selecting a subset of the bits and compresses them into a contiguous string of 20 bits in a second storage location 1004.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the address table reshuffling method of Melvin to the input address lookup engine of Chen, McAuley and Hunter for the purpose of providing a computationally and memory-efficient implementation of an address table for use in a network multiplexer as suggested by Melvin (col. 2 lines 16-19).

Claims 6, 14, 15, 20, 24, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and McAuley as applied to claim 1 above, in view of Goldberg et al. (Pub. No. US 2004/0013112 A1).

Claim 6, Chen teaches wherein the hash transformations on the apportioned address inputs are configured to be executed in parallel (Fig. 1, page 1 para. [0002]-[0005) referenced by the parallel Hardware Hash Functions 102 operating on the input address lookup request. Chen teaches the use of an XOR operation in determining a hash function output (page 3 para. [0048]-[0049]). Chen and McAuley do not teach execution in parallel within a single clock cycle such that the hash result is generated from the address input within the single cycle.

Goldberg teaches execution in parallel within a single clock cycle (page 5 para. [0070]) referenced by the parallel processing and performance within a single clock cycle, such that the hash result is generated from the address input within the single clock cycle

(page 6 para. [0074]-[0080]) referenced by the hash function using an XOR function and thus is performed within a single cycle.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of a single cycle clock XOR hash function of Goldberg to the input address lookup engine of Chen and McAuley for the purpose of dynamic packet filtering on the packets received over an input packet stream as suggested by Goldberg (Abstract lines 5-6).

Claim 14, Chen teaches wherein the hash transformations on the apportioned address inputs are configured to be executed in parallel (Fig. 1, page 1 para. [0002]-[0005]) referenced by the parallel Hardware Hash Functions 102 operating on the input address lookup request. Chen teaches the use of an XOR operation in determining a hash function output (page 3 para. [0048]-[0049]). Chen and McAuley do not teach execution in parallel within a single clock cycle such that the hash result is generated from the address input within the single cycle.

Goldberg teaches execution in parallel within a single clock cycle (page 5 para. [0070]) referenced by the parallel processing and performance within a single clock cycle, such that the hash result is generated from the address input within the single clock cycle (page 6 para. [0074]-[0080]) referenced by the hash function using an XOR function and thus is performed within a single cycle.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of a single cycle clock XOR hash function of Goldberg

to the input address lookup engine of Chen and McAuley for the purpose of dynamic packet filtering on the packets received over an input packet stream as suggested by Goldberg (Abstract lines 5-6).

Claim 15, Chen teaches a hash transformation. Chen and McAuley do not teach wherein the hash transformation system is implemented within a single hardware ASIC. Goldberg teaches wherein the transformation system is implemented within a single hardware ASIC (Fig. 24, page 12 para. [0149]-[0159]) referenced by the computing Platform 260 including an ASIC 264 to perform dynamic packet filtering.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of an ASIC core of Goldberg to the input address lookup engine of Chen and McAuley for the purpose of dynamic packet filtering on the packets received over an input packet stream as suggested by Goldberg (Abstract lines 5-6).

Claim 20, Chen teaches wherein the hash transformations on the divided address inputs are configured to be executed in parallel (Fig. 1, page 1 para. [0002]-[0005]) referenced by the parallel Hardware Hash Functions 102 operating on the input address lookup request. Chen teaches the use of an XOR operation in determining a hash function output (page 3 para. [0048]-[0049]). Chen and McAuley do not teach execution in parallel within a single clock cycle such that the hash result is generated from the address input within the single cycle.

Goldberg teaches execution in parallel within a single clock cycle (page 5 para. [0070]) referenced by the parallel processing and performance within a single clock cycle, such that the hash result is generated from the address input within the single clock cycle (page 6 para. [0074]-[0080]) referenced by the hash function using an XOR function and thus is performed within a single cycle.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of a single cycle clock XOR hash function of Goldberg to the input address lookup engine of Chen and McAuley for the purpose of dynamic packet filtering on the packets received over an input packet stream as suggested by Goldberg (Abstract lines 5-6).

Claim 24, Chen teaches a network device to perform a method for parallel hash transformation (Fig. 1, page 1 para. [0002]-[0005]) referenced by the network device using a lookup engine of N parallel Hardware Hash Functions 102, to generate a hash pointer (Fig. 1, page 1 para. [0005]) referenced by the N r-bit hash value outputs of the hardware hash functions, for an address input (Fig. 1, page 1 para. [0005]) referenced by the 97-bit layer-4 address <DA,SA,DP,SP,PRO>, the method comprising accessing an address input (Fig. 1, page 1 para. [0005]) referenced by the arrival of the address 101 for processing by the N different hardware hash functions 102, subdividing the address input into a plurality of portions (Fig. 3, Fig. 4, page 3 para. [0048]-[0049]) referenced by the Partition the address Step 302 for hashing by the parallel SHIFT/XOR operation for each segment by the Shift Control Logic 22, performing a hash

transformation on the portions in parallel (Fig. 3, Fig. 4, page 3 para. [0048]-[0049]) referenced by address segments input to the parallel hashing function of the Shift Control Logic 22, resulting in a corresponding plurality of hash portion outputs (Fig. 3) referenced by the output of the respective hashing Shift Control Logic units 22, and reassembling the hash portion outputs to generate a hash result corresponding to the address input (Fig. 3, page 3 para. [0048]-[0052]) referenced by the Selector 23 which receives the hashed outputs of the Shift Control Logic units 22 and selects the hashed output corresponding to the input address. Chen and McAuley do not teach a computer readable media having stored thereon computer readable code.

Goldberg teaches a computer readable media (Fig. 24, page 12 para. [0149]-[0150]) referenced by the RAM 270, having stored thereon computer readable code (Fig. 24, page 12 para. [0149]-[0150]) referenced by a computer operative to execute software adapted to perform packet filtering.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of the computing platform of Goldberg to the input address lookup engine of Chen for the purpose of dynamic packet filtering on the packets received over an input packet stream as suggested by Goldberg (Abstract lines 5-6).

Claim 25, Chen teaches wherein the hash transformation on the portions of the address input are performed in parallel using a plurality of processors (Fig. 1, page 1 para. [0005], Fig. 4, page 3 para. [0048]-[0049) referenced by the Hardware Hash units

120 1-N each performing a hash function on the respective address partitioned in step 302.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, McAuley and Donoghue as applied to claims 9, 10 above, and further in view of Hunter et al. (Pub. No. US 2002/0059197 A1).

Claim 12, Chen teaches wherein the input is configured to accept a layer-3 address input and the address input is respectively apportioned among the parallel hash units (Fig. 1, page 1 para. [0017]) referenced by the hashing mechanism adapted to a layer-3 router and the input address 101 is partitioned between parallel Hardware Hash units 102 1-N. Chen, McAuley and Donoghue do not teach the input address is a 128-bit address input.

Hunter teaches an input address is a 128-bit address input (page 1 para. [0006], page 2 para. [0035]) referenced by the Layer 3 address using the IP protocol which is 128-bit address for IPv6.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the 128-bit layer-3 address of Hunter to the input address lookup engine of Chen, McAuley and Donoghue for the purpose of locating an entry in a

forwarding database using an improved longest match search as suggested by Hunter (page 2 para. [0017]).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, McAuley, Donoghue and Hunter as applied to claims 9, 10, 12 above, and further in view of Melvin (Patent No. 6804767).

Claim 13, Chen, Donoghue and Hunter teach a lookup engine for network devices for MAC addresses and IP addresses. Chen, Donoghue and Hunter do not teach the hash result is a 20-bit hash result.

Melvin teaches a hash result is a 20-bit hash result (Fig. 10, col. 8 lines 34-54) referenced by the hash function selecting a subset of the bits and compresses them into a contiguous string of 20 bits in a second storage location 1004.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the address table reshuffling method of Melvin to the input address lookup engine of Chen, Donoghue and Hunter for the purpose of providing a computationally and memory-efficient implementation of an address table for use in a network multiplexer as suggested by Melvin (col. 2 lines 16-19).

Response to Arguments

The applicants arguments traversing the rejections of claims 1, 9, 19 have been fully considered. Chen does not teach the limitation "combining the hashing unit outputs to generate a hash result". An updated prior art search discloses McAuley teaches this limitation. McAuley teaches the use of masking address bits for processing through a hash memory array for output to a combination prioritizer. The rejection is revised to a 35 USC § 103(a) obvious combination of Chen and McAuley.

Regarding the arguments pertaining to the arrangement of the elements, the examiner respectfully disagrees. Chen teaches (Fig. 1) an address is input to a plurality of hash functions. This is further elaborated (Fig. 3) wherein the hash function is performed using shift control logic. The apportioning of the address (Fig. 1) is described in more detail by the parsing function (Fig. 4) wherein step 302 partitions the address.

Based on the prior art search, a revised round of rejections are presented.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L. Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JS

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